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(71) Applicant: TESSERA, INC. [US/US]; 3099 Orchard Drive, San Jose, CA 95134 (US).

(72) Inventors: NGUYEN, Tan; 1769 Laine Avenue, Santa Clara, CA 95051 (US). MITCHELL, Craig, S.; 3343 Geneva Drive, Santa Clara, CA 95051 (US). DISTEFANO, Thomas, H.; 16129 Greenwood Lane, Monte Sereno, CA 95030 (US).

(74) Agents: MILLET, Marcus, J. et al.; Lerner, David, Littenberg, Krumholz & Mentlik, LLP, 600 South Avenue West, Westfield, NJ 07090 (US).

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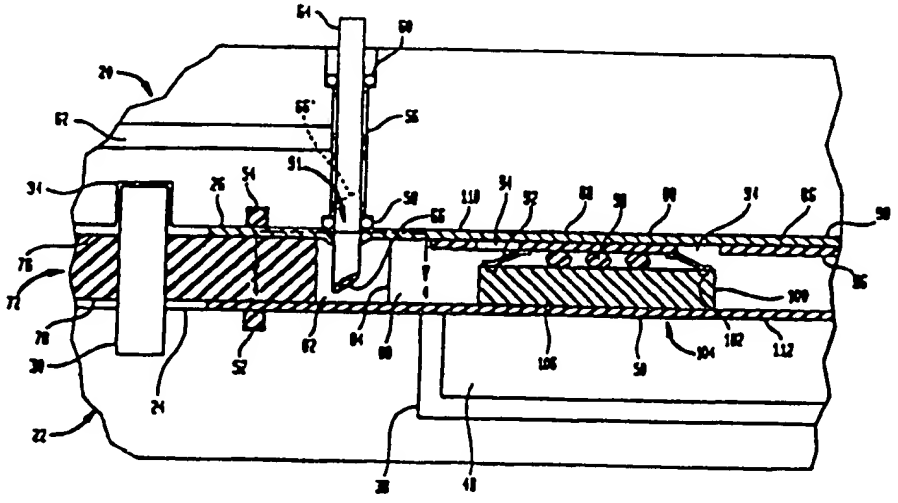
(54) Title: ENCAPSULATION OF MICROELECTRONIC ASSEMBLIES



(57) Abstract

Microelectronic assemblies are encapsulated using disposable frames (72). The microelectronic assemblies (104) are disposed within an aperture (80) defined by a frame. The aperture is covered by top and bottom sealing layers (110, 112) so that the frame and sealing layers define an enclosed space encompassing the assemblies. The encapsulant is injected into this closed space. The frame is then separated from the encapsulation fixture and held in a curing oven. After cure, the frame is cut apart and the individual assemblies are severed from another. Because the frame need not be held in the encapsulation fixture during curing, the process achieves a high throughput.

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Tech Insights

Exploring power-management design issues for advanced systems

MOSFETs Break Out Of The Shackles Of Wirebonding

By Replacing Wirebonds With A Copper Strap, Power MOSFETs Finally Enter A New Era Of Electrical And Thermal Efficiency.

Patrick Mannion

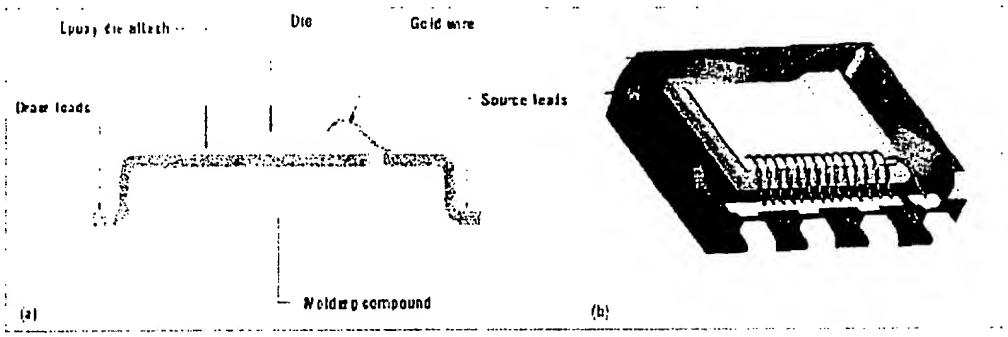
With processors, automotive electronics, and telecom board-mount applications all demanding greater power densities, thermally inefficient, high-resistance devices are wreaking havoc on system reliability. At the same time, power lost due to electrical inefficiency is draining valuable system resources. Add this to ongoing demands for lower cost, and it becomes apparent that traditional paths to efficiency nirvana are fast approaching diminishing returns. These paths, which follow the age-old practice of increasing silicon efficiency, have been so successful to date that the packaging and wirebond connections external to the die are now being recognized as the leading contributors to device inefficiency--not the die itself.

Recognizing this, International Rectifier, El Segundo, Calif., has replaced the wirebonds connecting the source to the leadframe with a solid copper strap that covers the surface of the die. This provides a highly conductive path, thermally and electrically, from the die to the leadframe and pc board. According to IR, this has resulted in a 10 to 20% reduction in thermal resistance and a 61% reduction in package contribution to electrical resistance for source connections. Called CopperStrap, the technology provides a 10 to 20% reduction in silicon temperature rise, allowing for less paralleling of MOSFETs, smaller chips and package outlines, and higher reliability.

Circumventing wwirebonding allows the CopperStrap to decrease assembly time and eliminates dreaded cratering and "purple plague" phenomena associated with wirebonds. Though not quantified as of yet, the connection methodology all but eliminates wirebond-related source inductance, a feature of

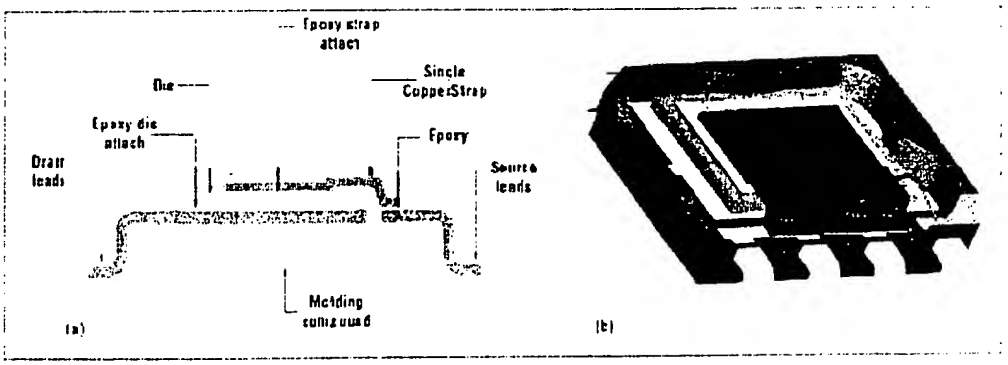
particular interest to buck-converter designers.

To date, MOSFET makers have managed to push silicon-die resistance into the single-digit milliohm range. But even this doesn't suffice. As a result, designers have been forced to opt for either a bigger, more expensive die in a larger package or for parallel arrays of less expensive devices that serve to reduce resistance, while spreading any generated heat around the board. Designs using either or both of these methods have been able to squeeze up to 10 A at 1.6 V from an input range of 10 to 21 V out of an SO-8 package. With upcoming designs looking for 15 A at 1.3 V from similarly sized or smaller packages, though, it becomes apparent that a new approach is necessary.



1. Traditional MOSFETs use wirebonding to attach the die to the source lead and the pc board (a). The wirebonds and top-metal-sheet resistance contribute about 90% of package resistance (b). Also, gold bonds are susceptible to voids, intermetallic formations, and parasitic inductance at high frequencies.

IR looked closely at all the elements that contribute to device resistance ***(Fig. 1a and b)***. In doing so, researchers realized that the wirebonds and top-metal-sheet resistance together contributed about 90% of the overall package resistance. The fourteen 2-mil gold wirebonds alone, already a maximum number for an SO-8 package, contributed about 1.1 m□. Replacing the wires with the CopperStrap reduced this to 0.11 m□ ***(Fig. 2a and b)***.



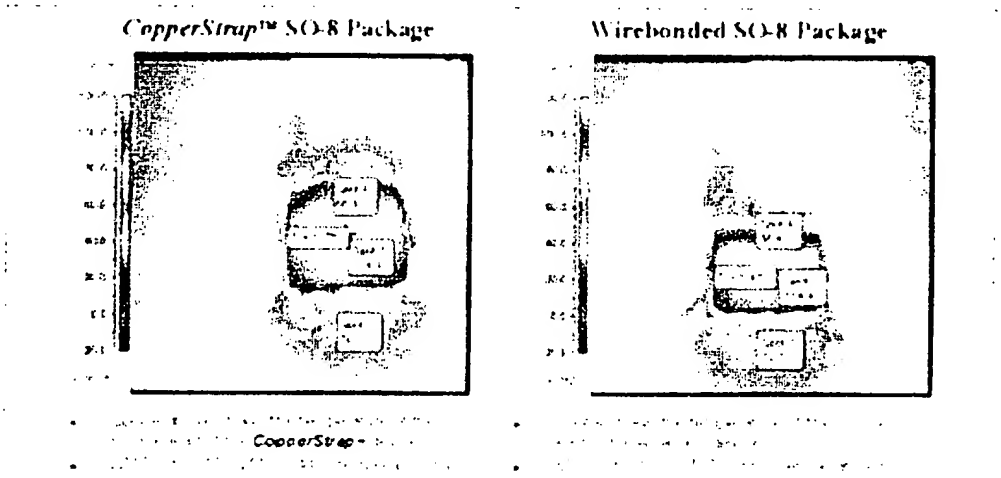
2. Replacing the fourteen 2-mil gold wirebonds (the maximum an SO-8 package can handle) with the CopperStrap reduced the die-source resistance from 1.1 m□ to 0.11 m□ (a). The top-metal resistance of the die shrank from 1.5 m□ to about 0.7 m□ (b).

The top-metal resistance of the die isn't normally taken into account when calculating package resistance, as it isn't considered to be part of the package. But depending on the location of the wirebonds on the top metal, 4 μm of aluminum could contribute as much as 1.5 m□. Placing the CopperStrap over most of the die's top surface provides a low-resistance parallel path, thereby reducing

the 1.5 mΩ to about 0.7 mΩ. That's a 61% reduction. If the die's top metal is much less than 4 µm, overall resistance savings could be even greater.

The implications for thermal management are even more interesting. Most of the heat from a power device in an SO-8 package is removed through a plate that forms the drain-lead connection on the back of the die. It's then conducted out to the copper in the pc board. Covering up to 70%, the top surface of the die with the copper sheet provides two thermal-dissipation avenues. The first is through the source leads to the pc board. The second takes advantage of the fact that the copper strap is routed closer to the top of the mold compound encapsulant than the traditional wirebonded solution. This allows heat to escape through radiation from the top surface of the package.

To get a better idea of how the CopperStrap theory plays out in practice, a thermograph was taken of two power MOSFETs in an SO-8 package ***(Fig. 3a and b)***. As can be seen from the image, the CopperStrap device does a much better job of conducting heat to the source leads, thereby taking it away from the die itself. This allows the device to deliver more power for a given device junction temperature.



3. A thermograph of two power MOSFETs in an SO-8, one with the CopperStrap (a) and one with wirebonding (b), shows how the CopperStrap device conducts more heat to the source leads, taking it away from the die. This allows the device to deliver more power for a given device junction temperature.

The CopperStrap's thermal capabilities can be put to maximum use in applications such as synchronous buck converters. Here, the low-side MOSFET's source connection is at ground potential. By increasing the thickness and area of the copper ground plane on the pc board, more heat can be pulled out of the die through the source pins.

CopperStrap has an extra advantage in buck converters. Its reduced source inductance is a result of wire elimination. But the degree to which performance has been improved hasn't been quantified yet.

On the reliability end, getting rid of the gold wire eliminates two major problems. First is wirebond cratering. It occurs when silicon fractures as a result of unoptimized wirebond parameters--the bonding force, as well as the intensity and duration of ultrasonic power. Cratering can't be detected reliably at final test. Therefore, it usually appears during reliability testing or in the field.

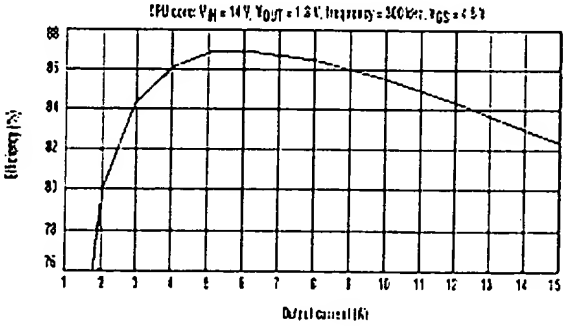
CopperStrap also puts an end to "purple plague." When gold is combined with an aluminum top metal, there's a risk of intermetallic formations. When exposed to high temperatures and/or small levels of

contaminants, the formations can be accelerated and can result in Kirkendall voids. These act in series with overall package resistance and can even result in complete open conditions. Purple plague can't be detected at final test, either. And once present, it can be very difficult to contain or control.

Other materials issues come into play. While copper is compatible with silver-filled epoxy and aluminum top metal, properties of the molding compound and silver-filled epoxy must be selected to optimize thermal, mechanical, and moisture resistance. Also,copper's expansion rate is different from that of gold wires. This has to be taken into account, especially when exposed to high solder-reflow temperatures and temperature cycling. The shape and features of the strap play a key role in how well stresses are distributed under these conditions.

KEY DEVICE PARAMETERS		
Parameter	**IRF7809**	**IRF7811**
V_{DS}	30 V	30 V
$R_{DS}(ON)TYP$	6m□	9m□
$Q_{G\ (TYP)}$	63 nC	18.2 nC
$Q_{SWITCH\ (TYP)}$	16.2 nC	5.8 nC
$R_{TH\ J\ LEAD\ (MAX)}$	20°C/W	20°C/W
$R_{TH\ J\ AMB\ (MAX)}$	35°C/W	35°C/W
Qswitch = $Q_{GS}2 + Q_{GD}$, where $Q_{GS}2$ = post gate-source threshold charge.		

CopperStrap is available in a dual chipset version: the high-side IRF7809, which uses PlanarFET technology, and the low-side TrenchFET-based IRF7809. Key performance specifications for these devices are shown **in the table**. The combination's ability to achieve efficiencies of up to 87% at 14 V_{IN}/1.3 V_{OUT}/6 A also is shown ***(Fig. 4)***. Efficiency falls off to about 83% at 15 A.



4. To date, the CopperStrap is capable of achieving efficiencies of up to 87% at 6 A. The efficiency falls off to about 83% at 15 A.

Cost per device is an extremely important facet of any product change or modification. In this case, there's no cost barrier, as the same manufacturing techniques and tooling can be used with minor adjustments. The only additional operation is the copper-strap placement, which can actually be incorporated into the existing die-attach operation.

Price And Availability

The IRF7809 and IRF7811 will be available in June as a chipset for $1.25 each per pair in 100,000-unit

quantities.

International Rectifier, Processor Power Group, 233 Kansas St., El Segundo, CA 90245; contact Carl Smith (310) 252-7968; fax (310) 252-7167; e-mail: csmith1@irf.com.

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Leadless Leadframe Package (LLP)

National Semiconductor
Application Note 1187
October 2002

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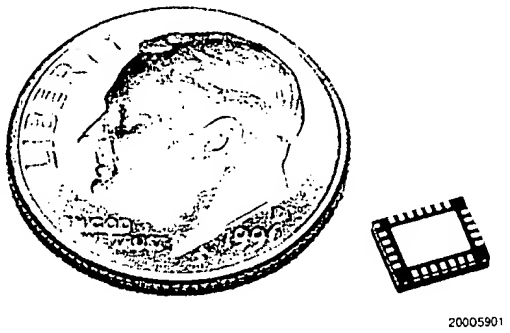

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FIGURE 1. 24 Pin LLP

Introduction

The Leadless Leadframe Package (LLP) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

Package Overview

KEY ATTRIBUTES

- Construction of the LLP is Illustrated in *Table 1*, *Figure 2*, and *Figure 3*.
- Terminal contacts:
  - — The contact pads (or solder pad) are located peripherally in single row, dual rows or in array format depending on the specific number of pins and body size.
  - — For certain specific applications the packages are incorporated with common power and/or ground pins as illustrated in *Figure 7*.
  - — All LLP contacts are plated with 85Sn/15Pb solder for ease of surface mount processing.
  - — All Lead-Free LLP contacts are plated with matt tin solder for ease of surface mount processing.
- Printed Circuit Board (PCB) footprint:
  - — National recommends a one-to-one correlation between the PCB land patterns and the package footprint.
  - — Soldering the exposed die attach pad (DAP) to the PCB provides the following advantages:
    - Optimizes thermal performance.
    - Enhances solder joint reliability.
    - Facilitates package self alignment to the PCB during reflow.
- The LLP is offered in either dual-in-line (DIP) or quad configuration.
- Coplanarity is not an area of concern for this package.
  - — All LLP contacts are flush with the bottom of the package.
- Moisture Sensitivity Level (MSL).
  - — All LLP packages are MSL 1 without the downbond. Specific package MSL can be confirmed via product application sheets.
  - — MSL of specific applications, requiring large packages, may vary depending on die size, exposed DAP design, and number of downbonds.

TABLE 1. Elements of the 24, 44 and 56 pin LLP

	24 Pin	44 Pin	56 Pin
Package Dimensions	5 x 4 x 0.8 mm	7 x 7 x 0.8 mm	9 x 9 x 0.8 mm
PCB Footprint Area (mm^2)	20	49	81
Standard	JEDEC	JEDEC	JEDEC
Pitch	0.5 mm	0.5 mm	0.5 mm
Weight	0.047 grams	0.104 grams	0.208 grams
Lead Frame	Copper	Copper	Copper
Lead Finish	Sn/Pb	Sn/Pb	Sn/Pb
Typical Thermal Resistance θ_{JA} (Note 1)	33°C/W	20°C/W	27°C/W (Note 2)

Note 1: The typical data reported are measured values at still air and 1 watt input power using four layer FR4 substrate with Vias and copper thickness of 2.0/1.0/1.0/2.0 oz.

Note 2: Package option with limited exposed pad size due to incorporations of ground and power rings.

Package Overview (Continued)

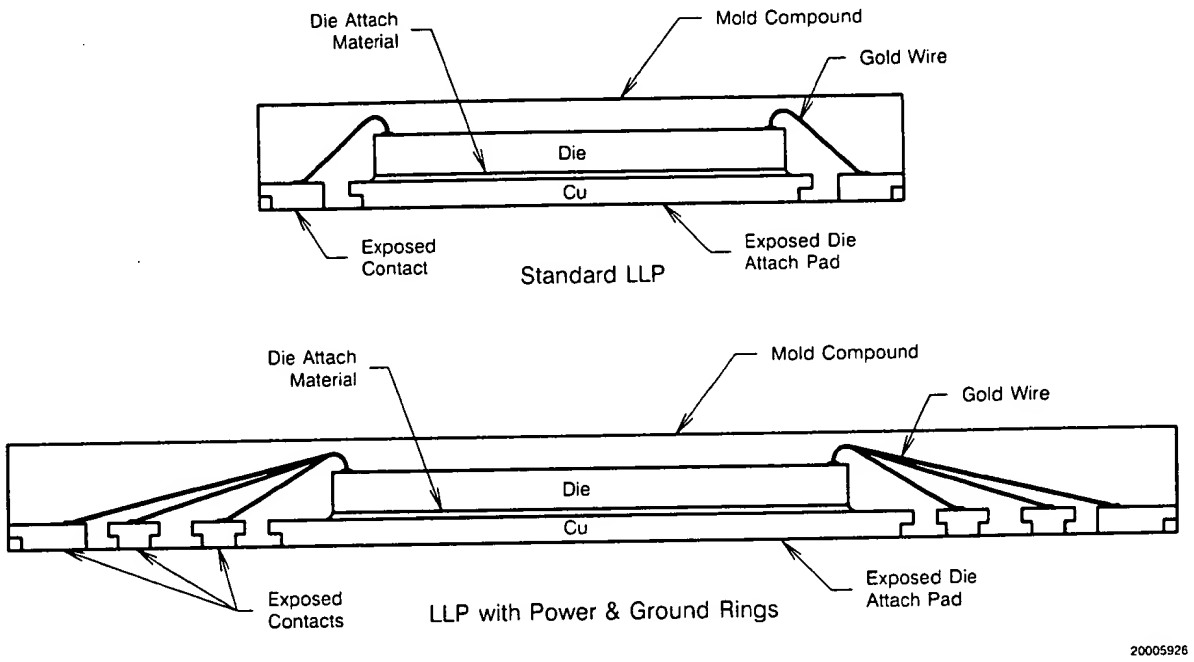


FIGURE 2. Construction of LLP

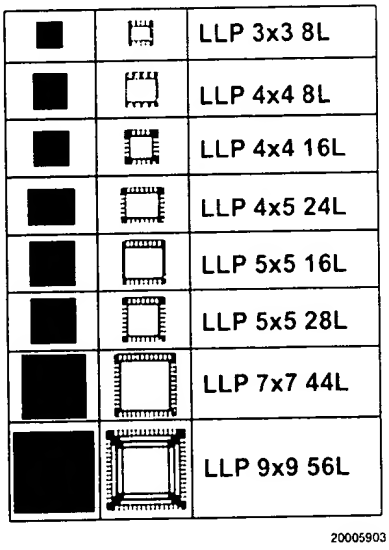


FIGURE 3. Examples

Package Overview (Continued)

PACKAGE OFFERING

Pin Count	Body size (mm)	Pitch (mm)	Max. Die Size (mm) (Note 5)	MKT DWG	MBS AD#	L/F Dwg #	QUAD/DIP (Note 4)	θ_{JA} (°C/W) (Note 3)
6	2.2 x 2.5	0.65	1.04 x 1.27	ldb06a	ldb006AA	36-1058-01	DIP	NA
6	2.92 x 3.29	0.65	1.45 x 1.85	lde06a	lde006AA	36-1056-01	DIP	NA
6	3.0 x 4.0	0.8	1.85 x 2.15	ldc06d	ldc006AE	36-0989-01	DIP	45.6
8	2.5 x 2.5	0.5	1.45 x 0.65	lda08b	lda008AC	36-1006-01	DIP	63.9
8	2.5 x 3.0	0.5	1.45 x 1.15	lda08c	lda008AD	36-1007-01	DIP	58.2
8	3.0 x 3.0	0.5	1.85 x 1.15	lda08a	lda008AA	36-0977-01	DIP	55.3
8	4.0 x 4.0	0.8	2.69 x 1.88	ldc08a	ldc008AA	36-0990-01	DIP	38.8
10	3.0 x 3.0	0.5	1.85 x 1.15	lda10a	lda010AA	36-1000-01	DIP	54.1
14	4.0 x 5.0	0.5	2.69 x 2.90	lda14b	lda014AB	36-1010-01	DIP	34.6
14	5.0 x 6.0	0.8	2.69 x 4.00	ldc14a	ldc014AA	36-1043-01	DIP	NA
16	4.0 x 4.0	0.5	2.13 x 2.13	lqa16a	lqa016AB	36-0978-02	QUAD	39.8
20	4.0 x 4.0	0.5	2.13 x 2.13	lqa20a	lqa020AB	36-1020-01	QUAD	38.7
24	5.0 x 4.0	0.5	2.10 x 3.10	lqa24a	lqa024AA	36-0973-01	QUAD	34.7
24	6.0 x 6.0	0.8	3.89 x 3.89	lqc24a	lqc024AA	36-1033-01	QUAD	NA
28	5.0 x 5.0	0.5	2.13 x 2.13	lqa28a	lqa028AA	36-0993-01	QUAD	30.8
32	5.0 x 6.0	0.5	2.13 x 2.13	lqa32b	lqa032AB	36-1031-01	QUAD	28.2
32	6.0 x 6.0	0.5	3.89 x 3.89	lqa32a	lqa032AA	36-1034-01	QUAD	26.4
44	7.0 x 7.0	0.5	4.00 x 4.00	lqa44a	lqa044AC	36-0976-03	QUAD	24.2
56	9.0 x 9.0	0.5	4.50 x 4.50	lqa56a	lqa056AA	36-1045-01	QUAD	NA

Note 3: 4-layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50 mm ground and power planes embedded in PCB

Note 4: DIP : Only two sides of the package have leads. QUAD: All four sides of the package have leads

Note 5: Maximum die size without downbond

PACKAGE HANDLING

The LLP is shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive (PSA) cover tape. The LLP is shipped in 7"" reels. Samples can be shipped in carrier tape format and/or trays.

Pin Count	Body Size (mm)	Marketing Drawing	Reel S/N	Tape Carrier S/N	Tape Cover S/N	Tray S/N
6	2.2 x 2.5	ldb06a	017983	078156	025360	NA
6	2.92 x 3.29	lde06a	017983	076263	025360	NA
6	3.0 x 4.0	ldc06d	017983	075537	025360	NA
8	2.5 x 2.5	lda08b	017983	075535	025360	NA
8	2.5 x 3.0	lda08c	017983	075536	025360	NA
8	3.0 x 3.0	lda08a	017983	073104	025360	075393
8	4.0 x 4.0	ldc08a	017983	073105	025360	075391
10	3.0 x 3.0	lda10a	017983	073104	025360	075393
14	4.0 x 5.0	lda14b	070376	075538	025360	NA
14	5.0 x 6.0	ldc14a	017982	075539	025361	NA
16	4.0 x 4.0	lqa16a	017983	073105	025360	075391
20	4.0 x 4.0	lqa20a	017983	073105	025360	075391
24	5.0 x 4.0	lqa24a	017983	073106	025360	NA
24	6.0 x 6.0	lqc24a	017982	075540	025361	NA
28	5.0 x 5.0	lqa28a	070376	073896	025360	075392
32	5.0 x 6.0	lqa32b	017982	075539	025361	NA
32	6.0 x 6.0	lqa32a	017982	075540	025361	NA

Package Overview (Continued)

Pin Count	Body Size (mm)	Marketing Drawing	Reel S/N	Tape Carrier S/N	Tape Cover S/N	Tray S/N
44	7.0 x 7.0	lqa44a	017982	073456 073107(alt) 077373(alt)	030137 025361(alt)	073329
56	9.0 x 9.0	lqa56a	023815	076519	025361	073320

JEDEC REGISTRATIONS

- Quad LLP Packages: MO-220
- Dual-in-line LLP Packages: MO-229

PCB Design Recommendations

NSMD VS. SMD LAND PATTERN

Two types of land patterns are used for surface mount packages: (1) Non-Solder Mask Defined Pads (NSMD) and (2) Solder Mask Defined Pads (SMD). NSMD has an opening that is larger than the pad, whereas SMD pads have a solder mask opening that is smaller than the metal pad. *Figure 4* Illustrates the two different types of pad geometry.

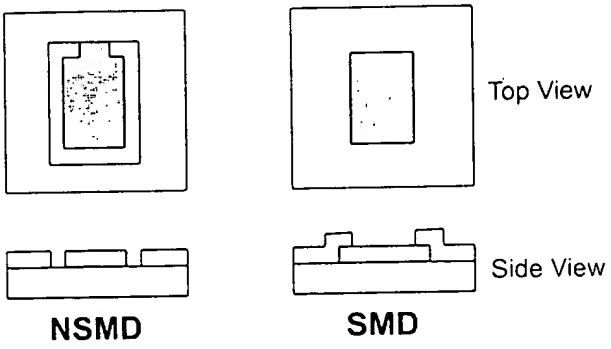


FIGURE 4. NSMD and SMD Pad Geometry

NSMD is preferred because the copper etch process has tighter control than the solder masking process. Moreover, the smaller size of the copper pad in the NSMD definition facilitates escape routing on the PCB when necessary.

NSMD pads require a ±0.075 mm (3 mils) clearance around the copper pad and solder mask this avoids overlap between the solder joint and solder mask and account for mask registration tolerances.

SMD pad definition can introduce stress concentration points near the solder mask on the PCB side. Extreme environmental conditions such as large temperature variations may cause fatigue that leads to cracked solder joints and reliability problems.

For optimal reliability, National recommends a 1:1 ratio between the package pad and the PCB pad for the LLP. If probing of signal pad is required, it is recommended to design probe pads adjacent to signal pads as shown in *Figure 5*. The trace between the signal pad and the probe pad must be covered by solder mask such that the requirement of 1:1 ratio of package pad to PCB pad is not violated. See *Figure 6* for PCB pad recommendations.

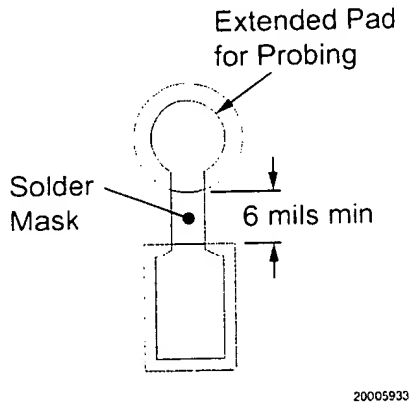
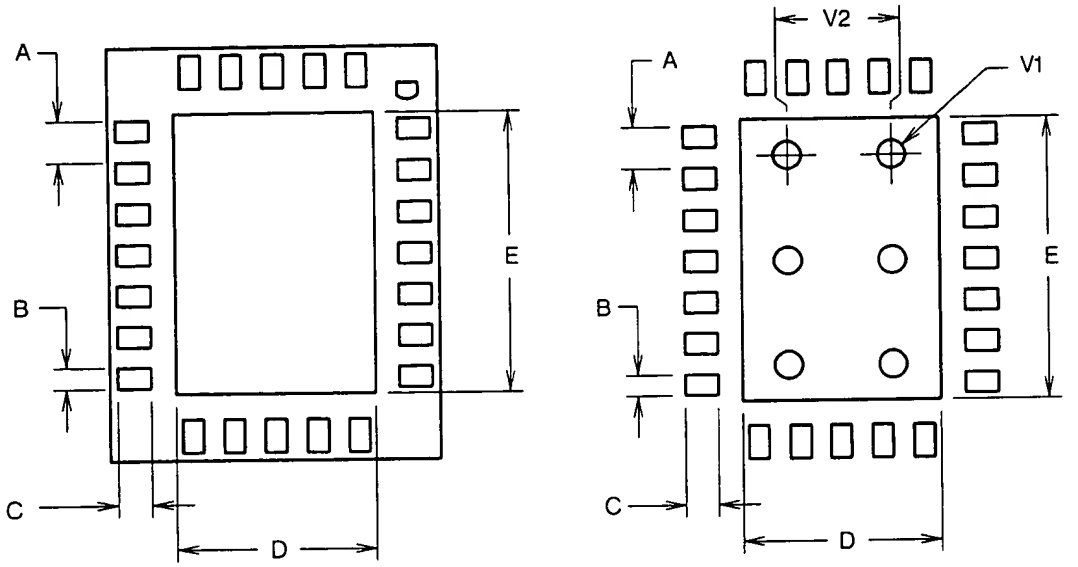


FIGURE 5. Recommended Pad Design for Probing

PCB Design Recommendations (Continued)



LLP Package Outline

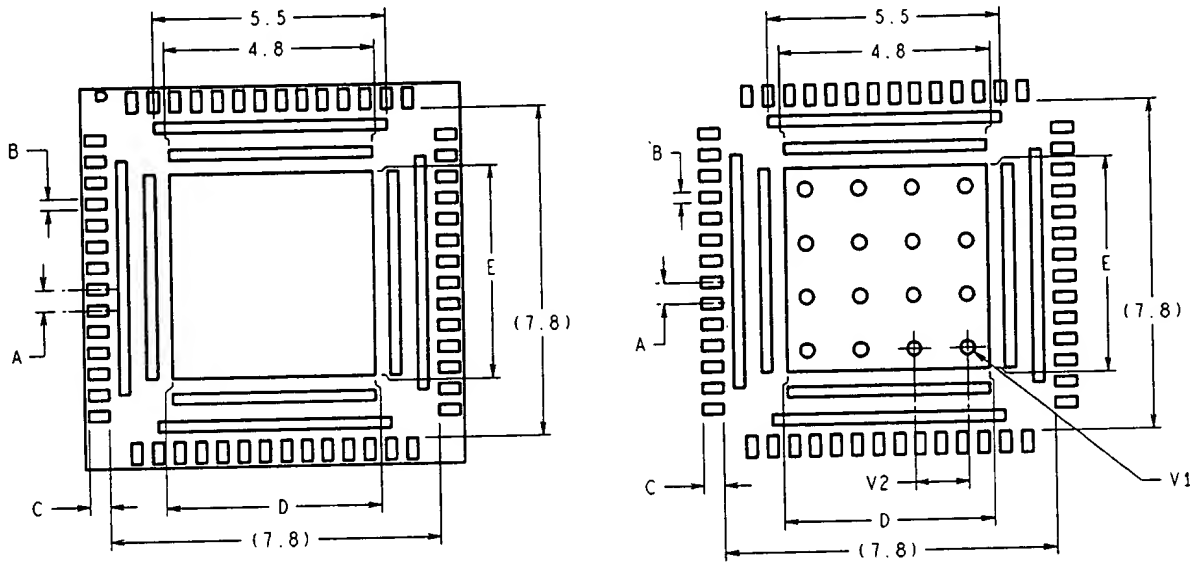
PCB Outline

20005907

Dimensions A, B, C, D, and E of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions refer to respective marketing outlines.
A - LLP Terminal Pitch
B - LLP Terminal Width
C - LLP Terminal Length
D - Exposed DAP Width
E - Exposed DAP Length
V1 - Thermal Via Diameter. Recommended 0.2 - 0.33 mm
V2 - Thermal Via Pitch. Recommended 1.27 mm

FIGURE 6. Typical Recommended Printed Circuit Board Dimensions

PCB Design Recommendations (Continued)



LLP Package Outline

PCB Outline

20005927

Number of pins	56
Package Size (mm)	9 x 9
A - LLP Terminal Pitch (mm)	0.5
B - LLP Terminal Width (mm)	0.25
C - LLP Terminal Length (mm)	0.5
D - Exposed DAP Width (mm)	4.8
E - Exposed DAP Length (mm)	4.8
V1 - Thermal Via Diameter (mm)	0.2 - 0.33
V2 - Thermal Via Pitch (mm)	1.27

FIGURE 7. Recommended Printed Circuit Board Dimensions for LLP 56 L with Ground and Power Bars.

THERMAL DESIGN CONSIDERATIONS

THERMAL LAND

The LLP thermal land is a metal (normally copper) region centrally located under the package and on top of the PCB. It has a rectangular or square shape and should match the dimensions of the exposed pad on the bottom of the package (1:1 ratio).

For certain high power applications, the PCB land may be modified to a "dog bone" shape that enhances thermal performance. The packages used with the "dog bone" lands will be a dual inline configuration. (See *Figure 8*).

PCB Design Recommendations

(Continued)

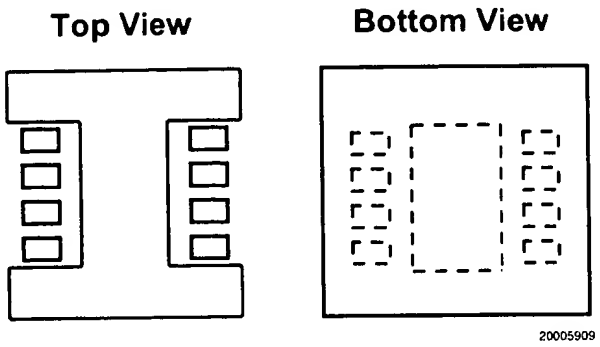


FIGURE 8. Dog Bone

THERMAL VIAS

Thermal vias are necessary. They conduct heat from the surface of the PCB to the ground plane. The number of vias is application specific and is dependent upon electrical requirements and power dissipation. A package thermal performance may be improved by increasing the number of vias. The improvement diminishes, however, as the number of vias increase. See *Figure 9*.

An array of vias with a 1.27 mm pitch is shown in *Figure 6*. The via diameter should be 0.2 mm to 0.33 mm with 1oz. copper via barrel plating. It is important to plug the via to avoid any solder wicking inside the via during the soldering process. If the copper plating does not plug the via, the thermal vias can be tented with solder mask on the top surface of the PCB. The solder mask diameter should be at least 75 microns (or 3 mils) larger than the via diameter. The solder mask thickness should be the same accross the entire PCB.

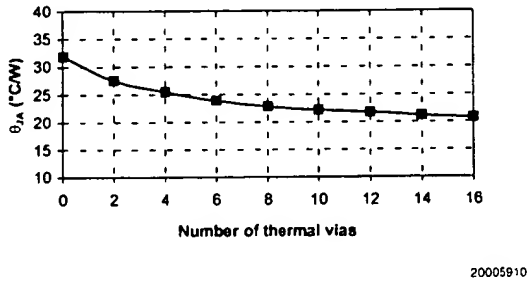


FIGURE 9. θ_{JA} vs. Number of Thermal Vias for the 44L LLP

EFFECTS OF THERMAL VOIDS

A void in the solder paste or die attach (generated during the manufacturing process) could have a direct impact on heat dissipation. The effect is not significant unless the void volume exceeds a certain percentage of the corresponding material volume (see *Figure 10*). **NOTE:** voids typically do not have an impact on reliability.

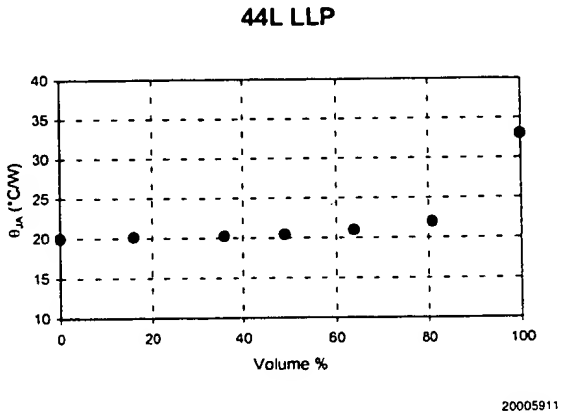


FIGURE 10. Thermal Voids Impact for the 44L LLP

THERMAL LAYERS IN THE PCB

Because of the small size and low profile, the majority of heat generated by the die within the LLP is dissipated through the exposed pad to PCB. Consequently, the PCB configuration and metal layers embedded in the PCB become important to achieving good thermal performance. In a 4-layer PCB (2 layers for signals and 2 layers for power/ground), the area of the embedded copper layer connecting to the thermal vias has significant effect on the thermal performance of the package. *Figure 11* shows simulation data of θ_{JA} vs. the embedded copper layer area for the 44L LLP. Increasing the copper layer area reduces the thermal resistance. However, in the similar manner, as the number of vias increases, the amount of thermal resistance improvement diminishes as the embedded copper area increases.

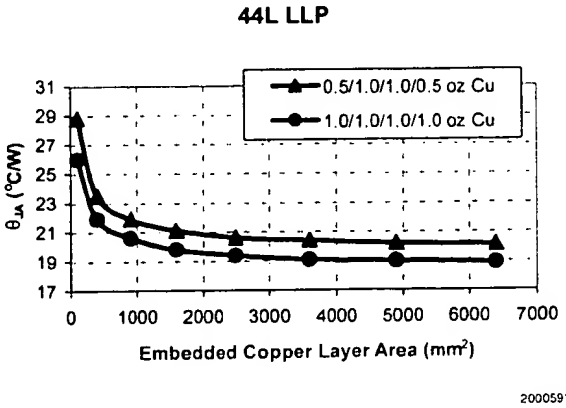


FIGURE 11. Effect of Thermal Layers on the 44L LLP's Junction-to-Ambient Thermal Resistance

SMT Assembly Recommendations

The LLP surface mount assembly operations include:

- PCB plating requirements
- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre reflow check - paste bridging
- Reflow and cleaning (dependent upon the flux type)
- X-ray post reflow check - solder bridging & Voids

PCB SURFACE FINISH REQUIREMENTS

A uniform PCB plating thickness is key for high assembly yield.

- For an electroless, nickel-immersion, gold finish, the gold thickness should range from 0.05 µm to 0.20 µm to avoid solder joint embrittlement.
- Using a PCB with **O**rganic **S**olderability **P**reservative coating (OSP) finish is also recommended, as an alternative to Ni-Au.
- For a PCB with Hot Air Solder Leveling (HASL) finish, the surface flatness should be controlled within 28 micron.

SOLDER STENCIL

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP package is highly recommended to improve board assembly yields.

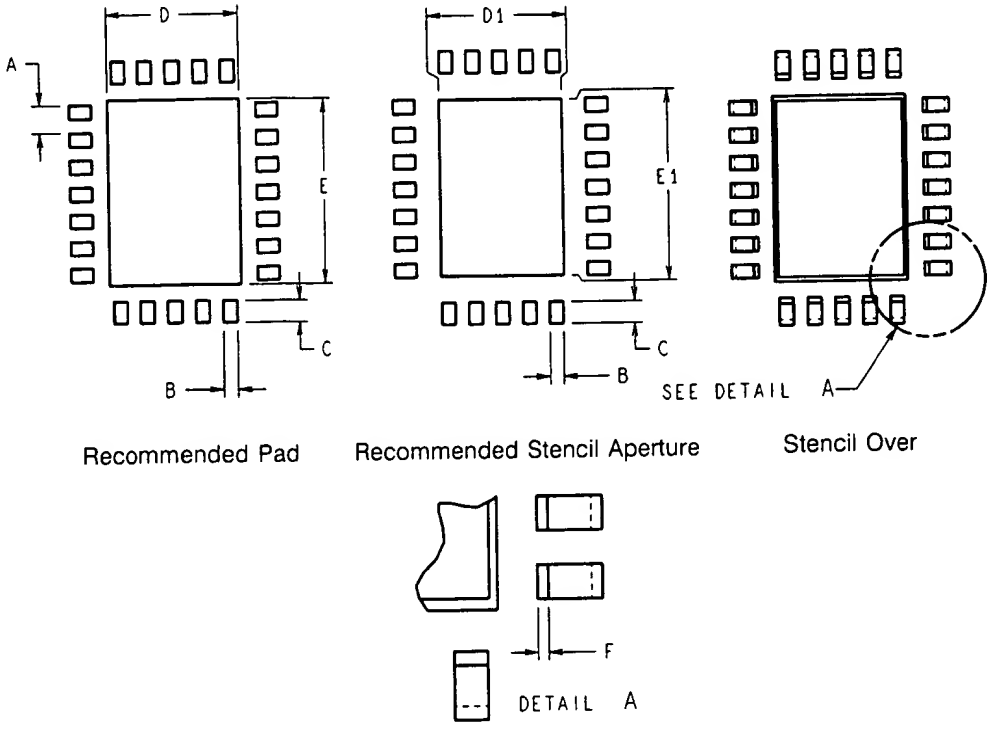
Stencils fabricated from chemical etching with elctro polished or laser cut is recommended. Tapered aperture walls (5˚ tapering) is recommended to facilitate paste release. Recommended stencil thickness is 127 µm. In order to prevent solder bridging the stencil aperture openings need to be modified as follows:

- The terminal contact aperture openings should be offset by 0.1 mm outward from the pads.
- For exposed pad aperture, up to 2 mm, the opening should be reduced to 95% of the corresponding PCB exposed DAP dimensions. See *Figure 12* and *Figure 13*.
- For exposed pad aperture with any side from 2 to 4 mm, the stencil opening should be split in two for any side. See *Figure 14*.
- For exposed pad aperature greater than 4 mm but without ground and power bars. See *Figure 15*.
- For exposed pad aperature greater than 4 mm with ground and power bars. See *Figure 16*.

TABLE 2. LLP Stencil Aperature Summary

Pin Count	MKT Dwg	I/O pad size	Pitch	DAP size	Stencil I/O	Aperature DAP	Dimension		
							D1	E1	H
6	ldb06a	0.25 X 0.4	0.65	1.2 X 0.75	0.25 X 0.4	*Figure 13*	1.1	0.7	N/A
6	ldc06d	0.3 X 0.5	0.8	2 X 2.2	0.3 X 0.5	*Figure 14*	0.85	0.85	0.3
6	lde06a	0.35 X 0.5	0.95	1.92 X 1.2	0.35 X 0.5	*Figure 13*	1.8	1.1	N/A
8	lda08a	0.25 X 0.5	0.5	1.8 X 1.2	0.25 X 0.5	*Figure 13*	1.7	1.1	N/A
8	lda08b	0.25 X 0.5	0.5	1.5 X 0.7	0.25 X 0.5	*Figure 13*	1.4	0.6	N/A
8	lda08c	0.25 X 0.5	0.5	1.5 x 1.2	0.25 X 0.5	*Figure 13*	1.4	1.1	N/A
8	ldc08a	0.3 X 0.5	0.8	3 X 2.2	0.3 X 0.5	*Figure 14*	1.25	0.85	0.3
10	lda10a	0.25 X 0.5	0.5	2 X 1.2	0.25 X 0.5	*Figure 13*	1.9	1.1	N/A
14	lda14b	0.25 X 0.5	0.5	3 X 3.2	0.25 X 0.5	*Figure 14*	1.25	1.35	0.3
14	ldc14a	0.4 X 0.5	0.8	4.35 X 3	0.4 X 0.5	*Figure 14*	1.925	1.25	0.3
16	lqa16a	0.25 X 0.5	0.5	2.2 X 2.2	0.25 X 0.5	*Figure 14*	0.85	0.85	0.3
20	lqa20a	0.25 X 0.5	0.5	2.2 X 2.2	0.25 X 0.5	*Figure 14*	0.85	0.85	0.3
24	lqa24a	0.25 X 0.4	0.5	3.4 X 2.4	0.25 x 0.4	*Figure 14*	1.45	0.95	0.3
24	lqc24a	0.3 X 0.5	0.8	4.2 X 4.2	0.3 X 0.5	*Figure 15*	0.5	0.5	0.3
28	lqa28a	0.25 X 0.5	0.5	3.2 X 3.2	0.25 X 0.5	*Figure 14*	1.35	1.35	0.3
32	lqa32a	0.25 X 0.5	0.5	4.2 X 4.2	0.25 X 0.5	*Figure 15*	0.5	0.5	0.3
32	lqa32b	0.25 X 0.5	0.5	4.2 X 3.2	0.25 X 0.5	*Figure 15*	0.5	0.5	0.3
44	lqa44a	0.25 X 0.5	0.5	4.3 X 4.3	0.25 X 0.5	*Figure 15*	0.5	0.5	0.3
56	lqa56a	0.25 X 0.5	0.5	4.8 X 4.8	0.25 X 0.5	*Figure 16*	0.5	0.5	0.3

SMT Assembly Recommendations (Continued)

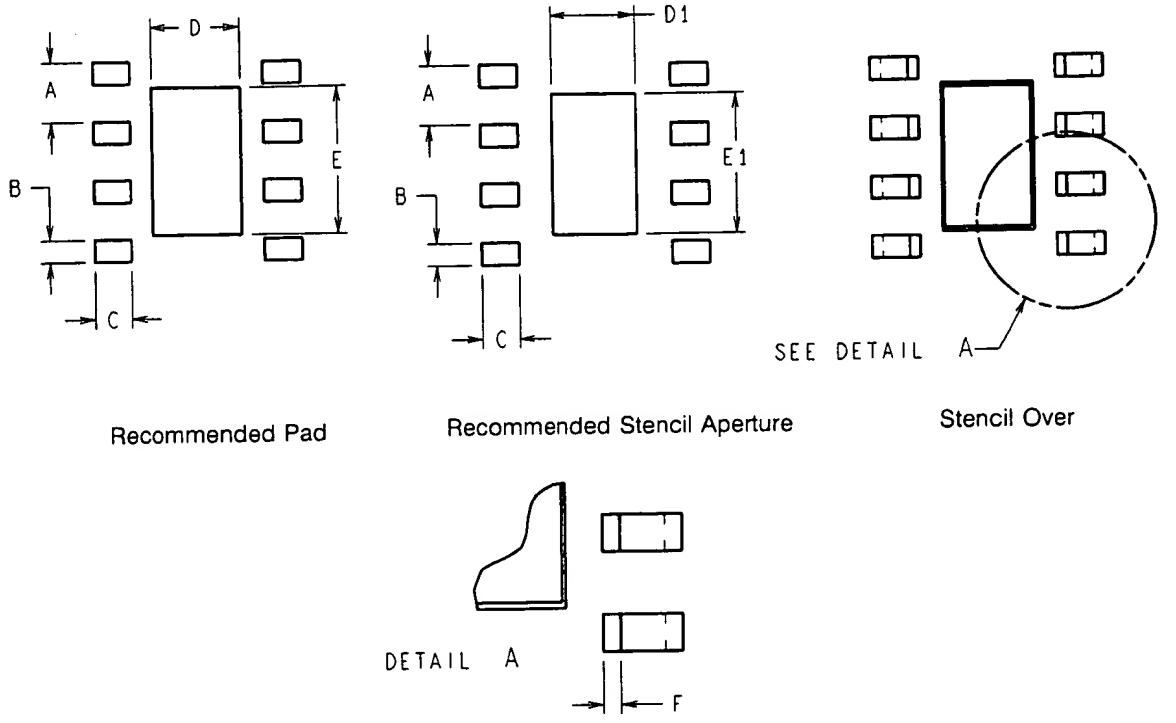


Recommended Pad Recommended Stencil Aperture Stencil Over

A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	0.95 x D
E1	0.95 x E
F	0.1 mm
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 12. Typical Recommended PCB Dimensions vs. Stencil Aperture for Quad Packages with DAP < 2 mm.

SMT Assembly Recommendations (Continued)

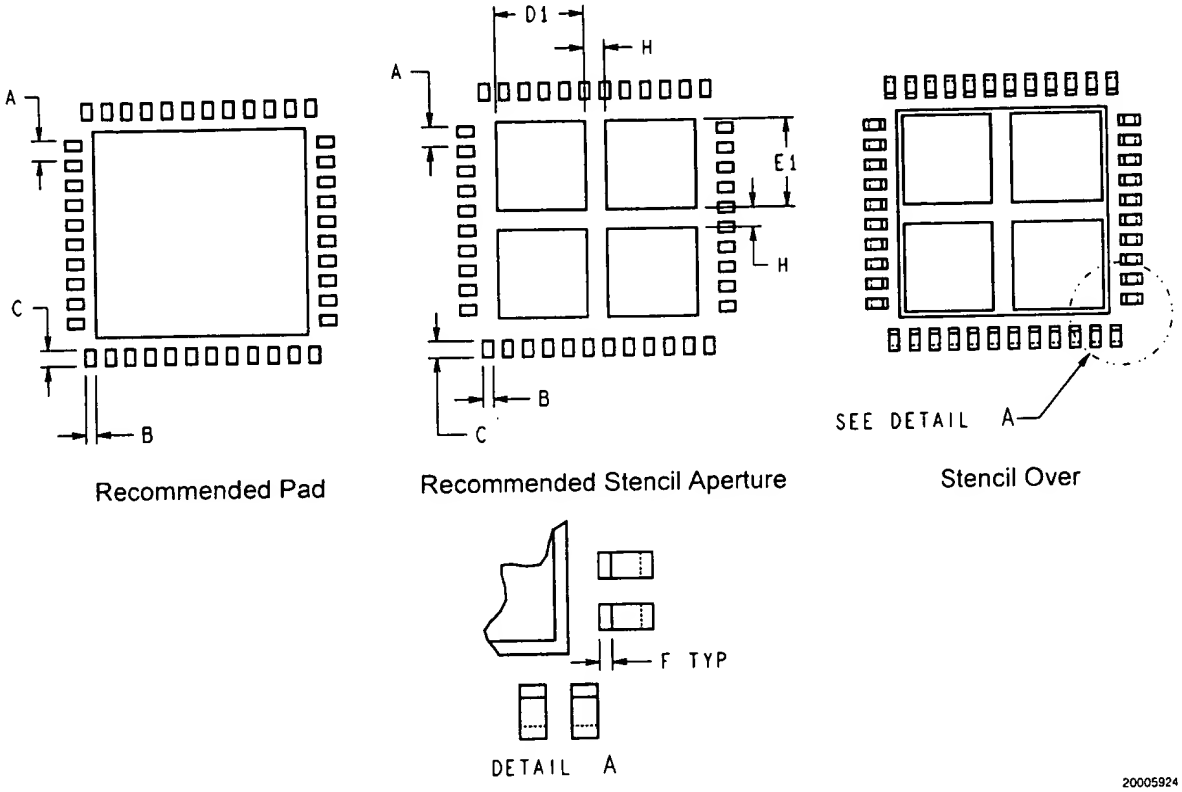


Recommended Pad | Recommended Stencil Aperture | Stencil Over

A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	0.95 x D
E1	0.95 x E
F	0.1 mm
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 13. Typical Recommended PCB Dimensions vs. Stencil Aperture for Dual In-line Packages with DAP < 2 mm.

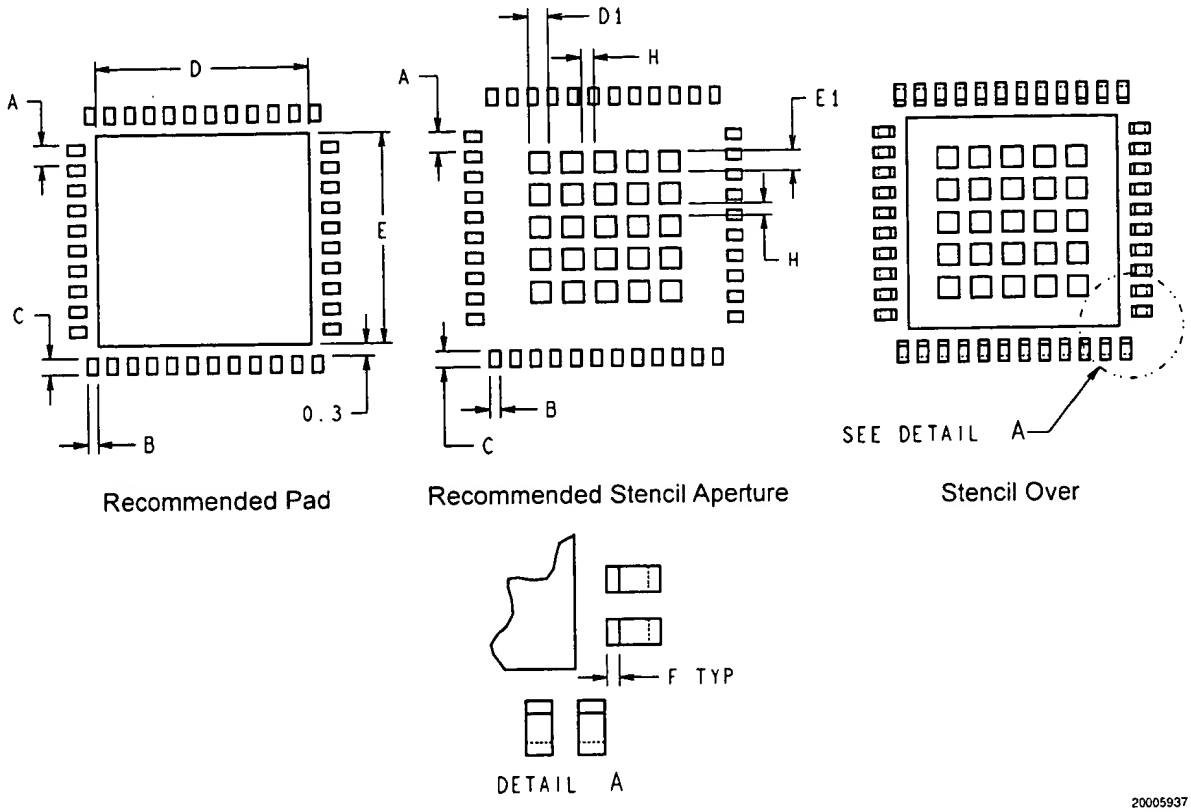
SMT Assembly Recommendations (Continued)



A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	See *Table 2*
E1	
F	
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 14. Typical Recommended Stencil Opening for Exposed DAP from 2 mm to 4 mm.

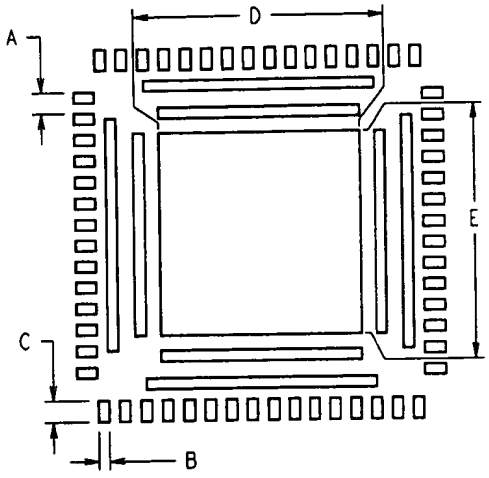
SMT Assembly Recommendations (Continued)



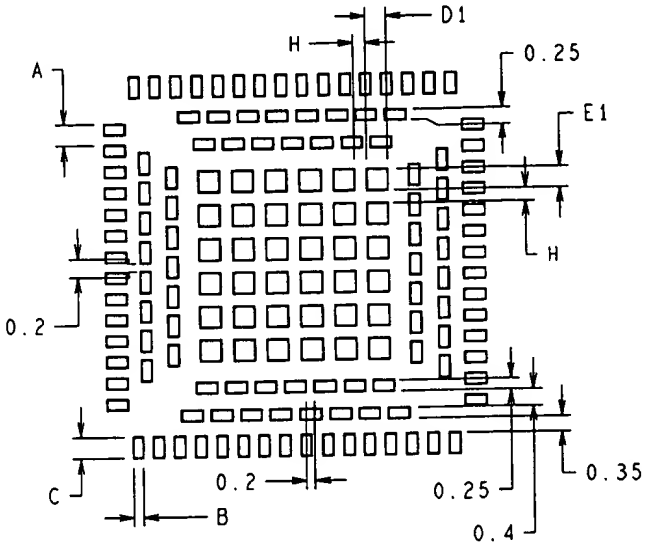
A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	See *Table 2*
E1	
F	
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 15. Typical Recommended Stencil Opening for Exposed DAP > 4 mm on any side without Ground and Power Bars.

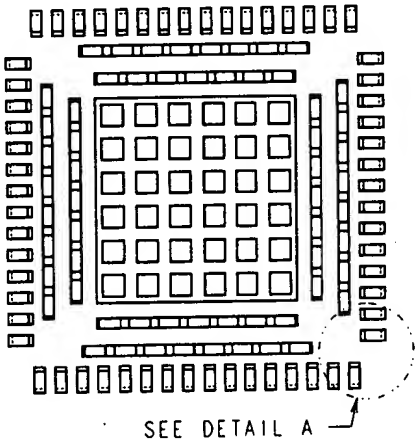
SMT Assembly Recommendations (Continued)



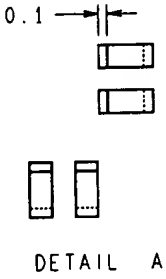
Recommended Pad



Recommended Stencil Aperture



Stencil Over



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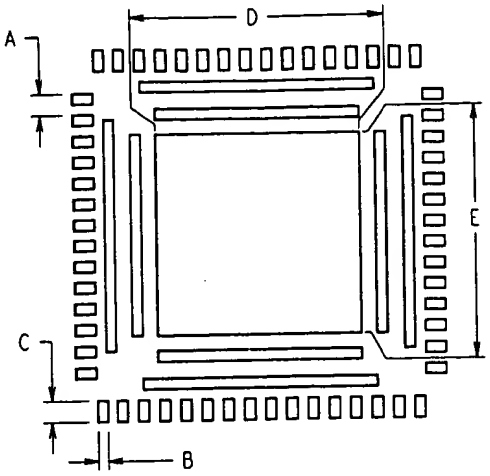
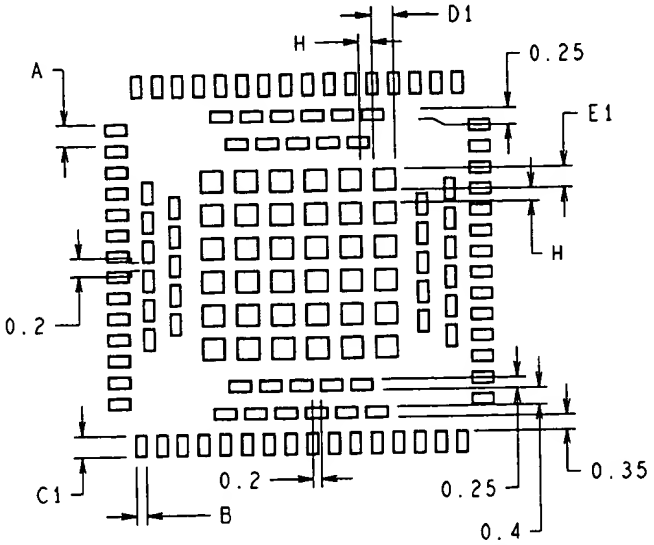
Number of pins	56
A - LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B - LLP, PCB, Stencil Terminal Width (mm)	0.25
C - LLP, PCB, Stencil Terminal Length (mm)	0.5
D - LLP, PCB Exposed DAP Width (mm)	4.8
D1 - Exposed DAP Aperture Width (mm)	0.5
H - Aperture split width, centered (mm)	0.3
E - LLP, PCB Exposed DAP Length (mm)	4.8
E1 - Exposed DAP Aperture Length (mm)	0.5
F - Stencil Aperture opening offset (mm)	0.1

FIGURE 16. Typical Recommended Stencil Opening for LLP with Exposed DAP, Ground and Power Bars.

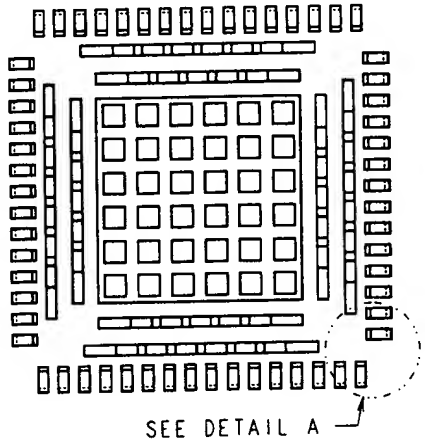
SMT Assembly Recommendations (Continued)



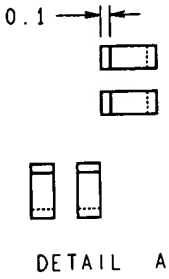
Recommended Pad



Recommended Stencil Aperture



Stencil Over



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Number of pins	56
A - LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B - LLP, PCB, Stencil Terminal Width (mm)	0.25
C - LLP, PCB Terminal Length (mm)	0.5
C1 - LLP Stencil Terminal Length (mm)	0.45
D - LLP, PCB Exposed DAP Width (mm)	4.8
D1 - Exposed DAP Aperture Width (mm)	0.5
H - Aperture split width, centered (mm)	0.3
E - LLP, PCB Exposed DAP Length (mm)	4.8
E1 - Exposed DAP Aperture Length (mm)	0.5
F - Stencil Aperture opening offset (mm)	0.1

FIGURE 17. Typical Recommended Stencil Opening for LLP with Exposed DAP, Ground and Power Bars for PCB with HASL Finish.

SMT Assembly Recommendations (Continued)

STENCIL OPENINGS FOR SOT23 5/6L FOOTPRINT COMPATIBLE LLP

- For the SOT23 5/6L footprint compatible LLP for which the PCB has been designed for the SOT23 package, refer to *Figure 18* for solder stencil openings.
- For new board design, it is recommended to use *Figure 13* for PCB pad and stencil openings.

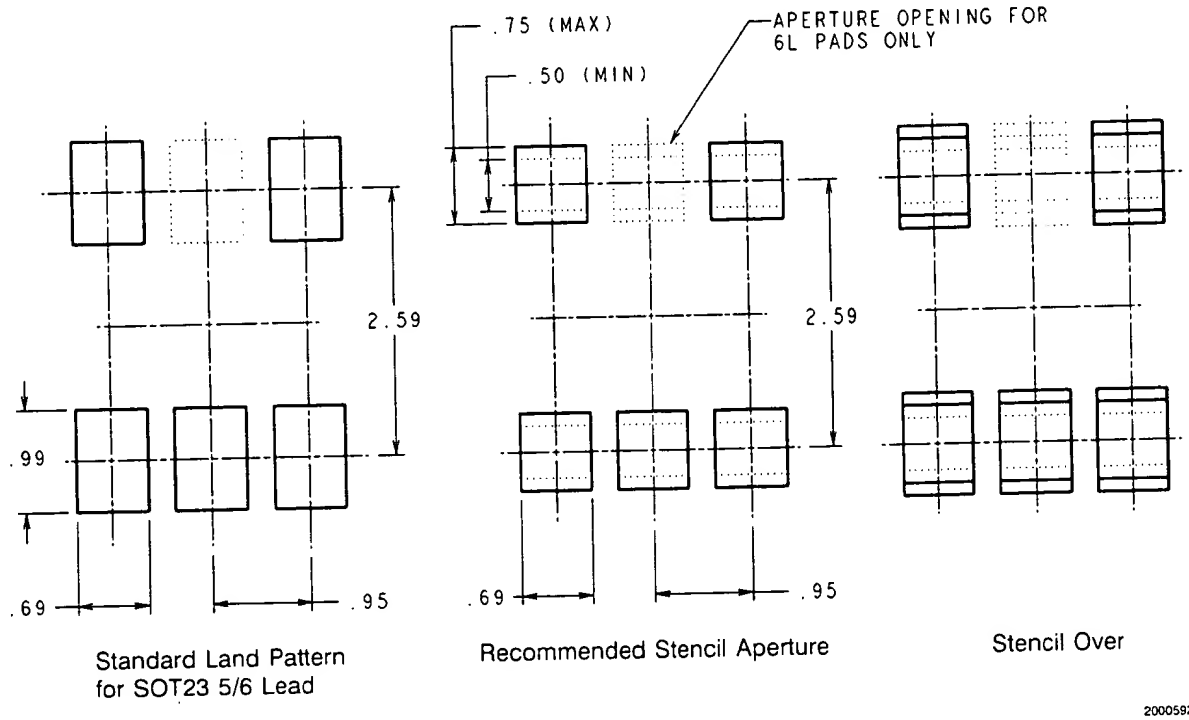


FIGURE 18. Recommended Stencil Aperture for SOT23 5/6 Lead Footprint Compatible LLP

PACKAGE PLACEMENT

LLP packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems are: (1) a vision system that locates a package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type renders more accurate place but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering feature of the LLP solder joint during solder reflow.

It is recommended to release the LLP package 1 to 2 mils into the solder paste.

SOLDER PASTE

Type 3, water soluble, no clean, and leadfree solder pastes are acceptable.

REFLOW AND CLEANING

The LLP may be assembled using standard IR / IR convection SMT reflow processes without any special considerations. As with other packages, the thermal profile for specific board locations must be determined. Nitrogen purge is recommended during solder for no-clean fluxes. The LLP is qualified for up to three reflow cycles at 235°C peak (J-STD-020). The actual temperature of the LLP is a function of:

- Component density
- Component location on the board
- Size of surrounding components

It is recommended that the temperature profile be checked at various locations on the board. *Figure 19* and *Figure 20* illustrate typical reflow profiles.

SMT Assembly Recommendations (Continued)

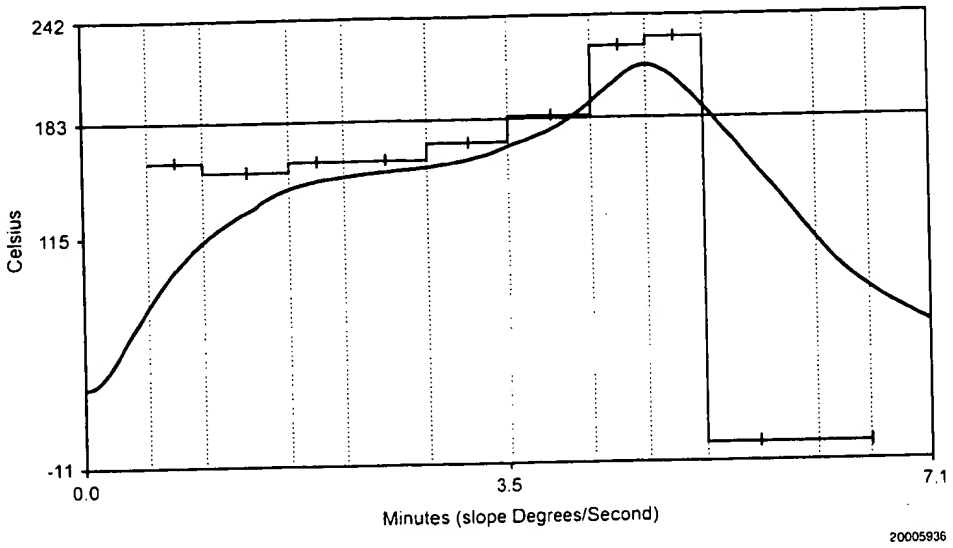


FIGURE 19. Typical Reflow Profile

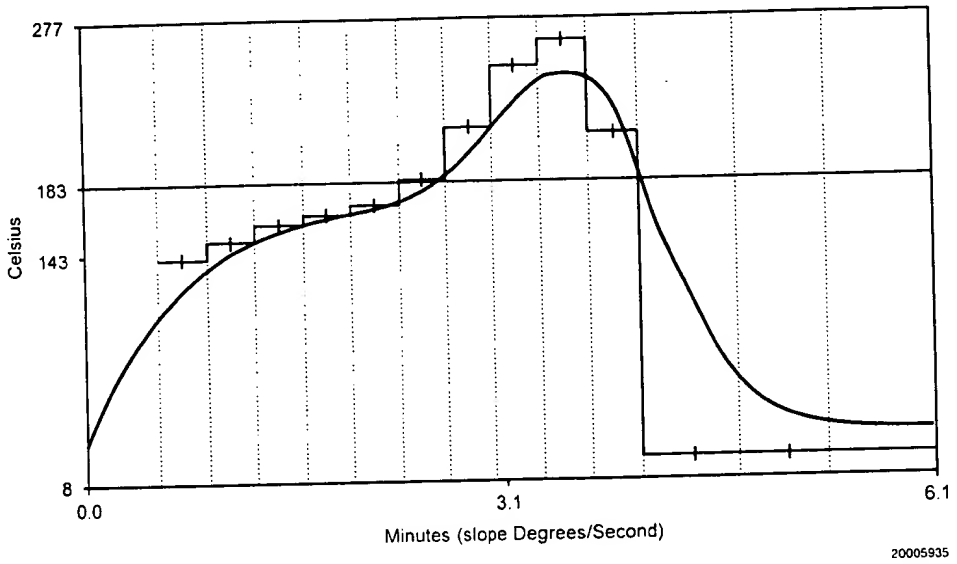
		Convection / IR
Ramp Up °C/sec (Note 8)	Maximum	4°C/sec
	Recommended	**2°C/sec** (Note 6)
	Minimum	(Note 7)
Dwell Time ≥ 183°C (Note 8)	Maximum	85 seconds
	Recommended	**75 seconds** (Note 6)
	Minimum	(Note 7)
Peak Temperature (Note 8)	Maximum	240°C
	Recommended	**215°C**
	Minimum	(Note 7)
Dwell Time Max. (within 5°C of peak temperature)	Maximum	10 seconds
	Recommended	**5 seconds**
	Minimum	1 second
Ramp Down °C/sec (Note 8)	Maximum	4°C/sec
	Recommended	**2°C/sec**
	Minimum	(Note 7)

Note 6: Will vary depending on board density, geometry, and package types. May vary depending on solder paste manufactures recommendations.

Note 7: Will vary depending on package types, and board density.

Note 8: All Temperatures are measured at the PCB surface.

SMT Assembly Recommendations (Continued)



Note : For detail settings, please refer to solder paste manufacturer's recommendation.

FIGURE 20. Typical Reflow Profile - Lead Free

SOLDER JOINT INSPECTION

After surface mount assembly, transmission X-ray should be used for **sample** monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens and voids. **NOTE:** voids typically do not have an impact on reliability. *Figure 21* shows a typical X-ray photograph after assembly.

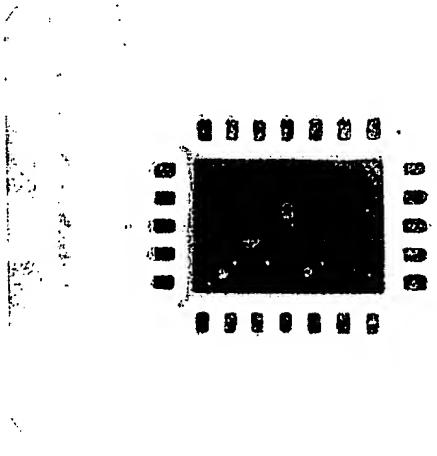


FIGURE 21. Typical X-ray after process

In the process setup, it is recommended to use side view inspection in addition to X-ray to determine if there are 'Hour Glass' shaped solder existing. The 'Hour Glass' solder shape is is not a reliable joint. 90° mirror projection can be used for side view inspection.

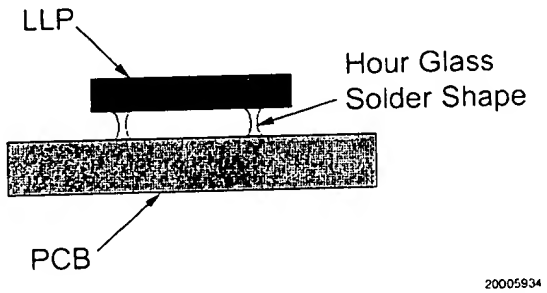


FIGURE 22.

REPLACEMENT/ REWORK

The quality of the rework is controlled by:

- Directing the thermal energy through the component body to solder without over-heating the adjacent components.
- Heating should occur in an encapsulated, inert, gas-purged environment where the temperature gradients do not exceed ±5°C across the heating zone.
- Using a convective bottom side pre-heater to maximize temperature uniformity.

SMT Assembly Recommendations

(Continued)

- Interchangeable nozzles designed with different geometries will accommodate different applications to direct the airflow path

NOTE: Standard SMT rework systems are capable of these elements.

Removal of the LLP Removing the LLP from the PCB involves heating the solder joints above the liquidus temperature of eutectic (63Sn-37Pb) solder using a vacuum gas nozzle. Baking the PCB at 125°C for 4 hours is recommended PRIOR to any rework. Doing this removes any residual moisture from the system, preventing moisture induced cracking or PCB delamination during the demount process.

A 1.27 mm (50 mil) keep-out zone for adjacent components is recommended for standard rework processing. If the adjacent components are closer than 1.27 mm, custom tools are required for the removal and rework of the package.

It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100°C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, nozzle vacuum is automatically activated and the component is removed. After removing the package, the pads may be heated with the nozzle to reflow any residual solder, which may be removed using a Teflon tipped vacuum wand.

Site Preparation Once the LLP is removed, the site must be cleaned in preparation for package attachment. The best results are achieved with a low-temperature, blade-style conductive tool matching the footprint area of the LLP in conjunction with a de-soldering braid. No-clean flux is needed throughout the entire rework process. Care must be taken to avoid burn, lift-off, or damage of the PCB attachment area. See *Figure 23*.

Solder Paste Deposition Because the LLP is a land area type package, solder paste is required to insure proper solder joint formation after rework. A 127 µm (5 mil) thick mini-stencil is recommended to deposit the solder paste patterns prior to replacement of the LLP. See *Figure 24*.

Component Placement Most CSP rework stations will have a pick and place feature for accurate placement and alignment. Manual pick and place, with only eye-ball alignment, is not recommended. It is difficult or impossible to achieve consistent placement accuracy.

Component Reflow It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100°C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, the solder will reflow and the LLP will self align. *Figure 25* shows a cross section of a solder joint after rework.

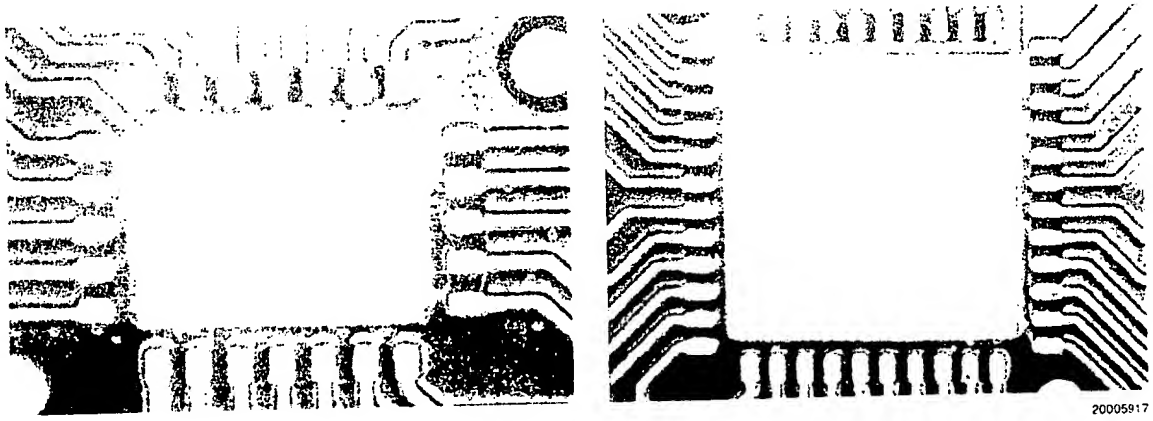


FIGURE 23. Pads After Removing Components and Cleaning

SMT Assembly Recommendations (Continued)

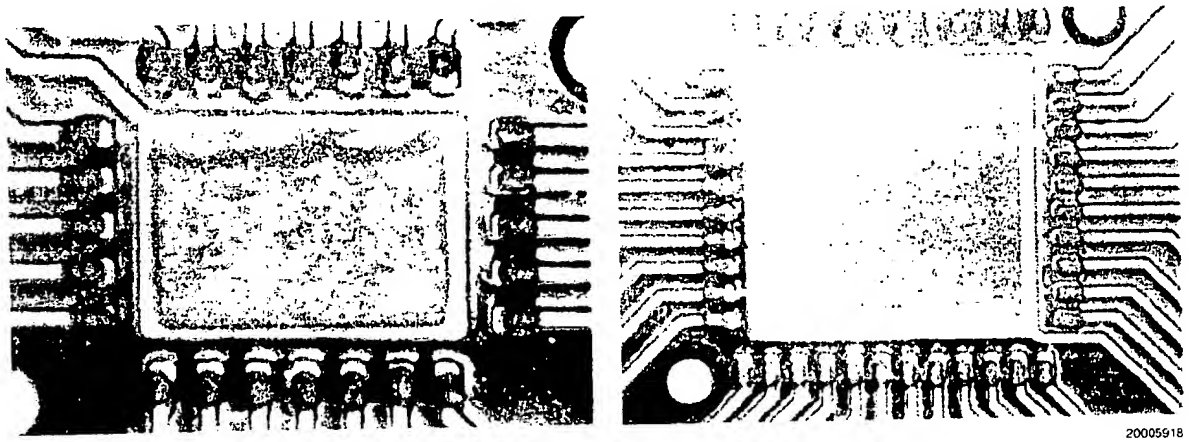


FIGURE 24. Solder Paste Printing of LLP 24 and LLP 44 Using 127 µm (5 mil) Thick Stencil

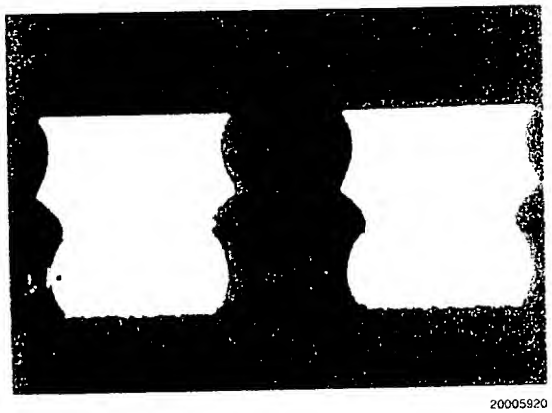


FIGURE 25. X-section Across Solder Joints

Appendices

APPENDIX 1: BOARD LEVEL RELIABILITY TEST DATA

Temperature Cycle Test

Test Conditions:

- Temperature Range: −40 to 125˚C
- Cycle Duration: 1 hour (15 minute ramp/15 minute Dwell)
- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Test Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit

Failure Determination: Change of 10% in Net Resistance

Results:

24L 4 mm x 5 mm LLP Package
(Package Die Attach Pad soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/41	0/84	0/83
500 Cycles	0/41	0/84	0/83
1050 Cycles	0/41		

24L 4 mm x 5 mm LLP Package
(Package Die Attach Pad NOT soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/81	0/78	0/76
500 Cycles	0/81	0/78	0/76
950 Cycles	0/81	0/78	0/76
1050 Cycles	0/81	0/78	0/76

44L 7 mm x 7 mm LLP Package
(Package Die Attach Pad soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/33	0/69	0/88
500 Cycles	0/33	0/69	0/88
1050 Cycles	0/33	0/69	0/88

44L 7 mm x 7 mm LLP Package
(Package Die Attach Pad NOT soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/81	0/78	0/76

Appendices (Continued)

Timepoint	Lot A	Lot B	Lot C
500 Cycles	0/81	0/78	0/76
950 Cycles	0/81	0/78	0/76
1050 Cycles	0/81	0/78	0/76

Standard 56L 9 mm x 9 mm Package
(Power and Ground Ring not soldered to the PCB)

Timepoint	Results
0 Cycles	0/75
500 Cycles	0/75
1050 Cycles	0/75

Lead-Free 56L 9 mm x 9 mm Package
(Power and Ground Ringsoldered to the PCB with SnAgCu solder paste and Sn lead finish)

PCB Finish	750 TMCL	1050 TMCL
NiAu	0/98	0/98
OSP	0/96	0/96

Standard & Lead-Free 56L LLP Board Level TMCL Comparison

Lead Finish	Solder Paste	PCB Finish	750 TMCL	1050 TMCL
Sn	SnPb	NiAu	0/100	0/100
SnPb	SnPb	NiAu	0/100	0/100
Sn	SnPb	OSP	0/99	0/99
SnPb	SnPb	OSP	0/95	0/95
Sn	SnAgCu	NiAu	0/98	0/98
SnPb	SnAgCu	NiAu	0/99	0/99
Sn	SnAgCu	OSP	0/96	0/96

SOT23 5/6L Footprint Compatible LLP

Timepoint	DAP soldered to PCB	DAP not soldered to PCB
0 cycles	0/126	0/84
500 cycles	0/126	0/84
1050 cycles	0/126	0/84

14 Lead Power LLP

Timepoint	Results
0 Cycles	0/80
500 Cycles	0/80
1050 Cycles	0/80

Board Drop Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 2 - 5 micro inches thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Cumulative Dead weight of the board: 150 Grams
- Drop Height: 1.5 meters
- Drop Surface: Non cushioning vinyl tile
- Number of Drops: 30 total
  - — 7 drops: along the length of the PCB
  - — 7 drops: along the width of the PCB
  - — 8 Drops: Along the diagonal of the board
  - — 8 Drops: With the components on the top of the board

Failure Determination: Change of 10% in Net Resistance

Results:

Package Type	Drop Test Results
24L 4 mm x 5 mm LLP (DAP soldered to PCB)	0/20
24L 4 mm x 5 mm LLP (DAP NOT soldered to PCB)	0/20
44L 7 mm x 7 mm LLP (DAP soldered to PCB)	0/20
44L 7 mm x 7 mm LLP (DAP NOT soldered to PCB)	0/20
56L 9 mm x 9 mm LLP (DAP soldered, Power/Ground Rings soldered to PCB)	0/25
14L Power LLP	0/32

Vibration Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Die attach pad soldered to PCB
- Vibration test conditions:
  - — Sinusoidal excitation performed for 1 hour at 20G force followed by 3 hours at 40G force
  - — Random Vibration with variable frequencies ranging from 20Hz to 2,000Hz for 3 hours with a force of 2G RMS

Results: DAP Soldered to PCB

Package Type	Test Results
24L 4 mm x 5 mm LLP	0/24
44L 7 mm x 7 mm LLP	0/20
56L 9 mm x 9 mm LLP	0/25
14L 6 mm x 5 mm Power LLP	0/32

APPENDIX 2: THERMAL SIMULATION DATA FOR POWER LLP

Thermal Simulation Conditions

All dimensions are in millimeters

Appendices (Continued)

Thermal Simulation Conditions (Continued)

Die Size	4.09 x 2.67 x 0.216
DAP Size	4.35 x 3.00
Package Size	6.00 x 5.00 x 1.00
Thermal Vias	0, 2, 4, 8, 12. See *Figure 26.*
Board Size	101.6 x 76.2 x 1.6 (4 layer JEDEC)
Copper Thickness	2.0/1.0/1.0/2.0 oz. (1 oz. = 36 µm)
Copper Coverage	Top layer: traces (27.5 x 0.25) plus metalization area as shown in *Figure 27.* Middle layers: 60.0 x 60.0 Bottom layer: 15% of the board area.

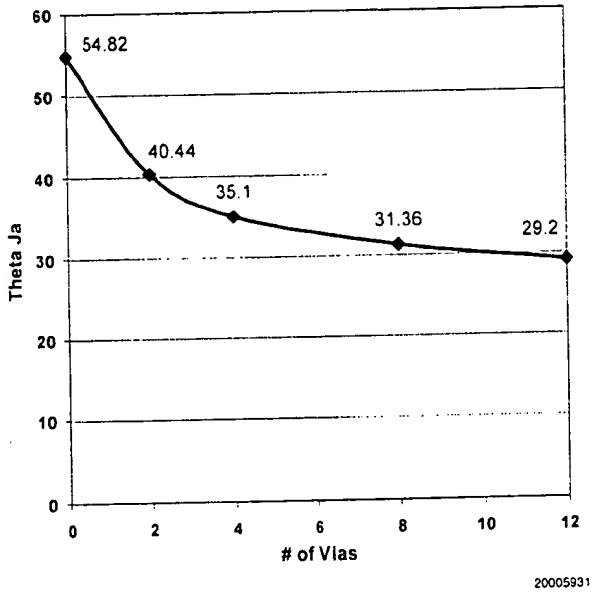


FIGURE 26. θ_{JA} as a Function of Number of Vias Placed in PCB

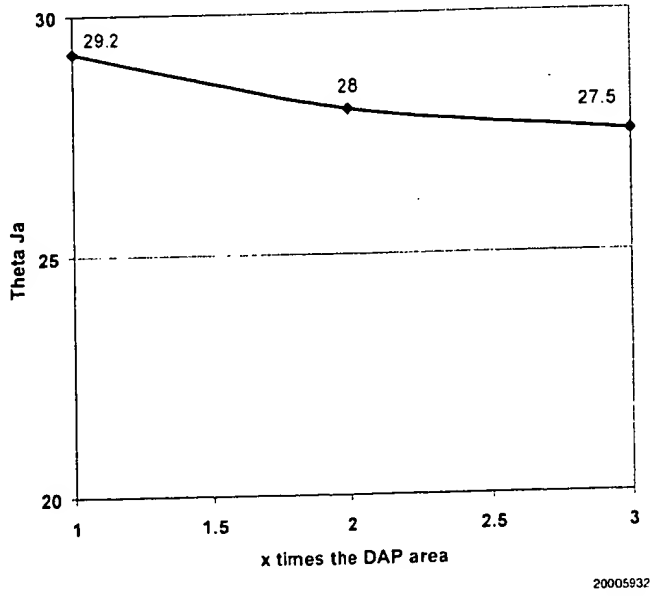


FIGURE 27. θ_{JA} as a Function of Top Metalization Area

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News

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Contact: Bob Decker, Wall Street Communications
Phone: 650-323-3936 Fax: 650-323-5650
Email: Bob.Decker@wallstcom.com

4 milliohms in the SO-8: Vishay Siliconix Sets New Record For Power MOSFET On-Resistance

New Package Technology Yields Nearly Twofold Improvement Over Previous State-of-the-Art

SANTA CLARA, CALIFORNIA - December 9, 1998 - Vishay Siliconix today announced a major breakthrough in power MOSFET performance with the release of an n-channel device offering maximum on-resistance of just 4 milliohms in the SO-8 package. The new Si4430DY is one of three new LITTLE FOOT® devices that combine Vishay Siliconix's 32-million cell TrenchFET® silicon with an advanced technique that dramatically reduces the packaging contribution to overall device resistance.

"With our 32 million cells per square inch TrenchFET technology, which remains the state of the art for power MOSFETs, Vishay Siliconix power MOSFETs reached the point where approximately half the total on-resistance for an SO-8 device was in the package components rather than the silicon," said Dr. Felix Zandman, Chairman of the Board and CEO of Vishay Intertechnology, Inc. "The next logical step was to reduce the resistance of the package itself, which is what we have done in these new LITTLE FOOT devices, with dramatic results."

To create these new LITTLE FOOT devices, Vishay Siliconix has developed a proprietary PowerConnect™ technology to replace the bond wires found in traditional power MOSFET packages with a direct connection between the silicon die and the copper lead frame. The result is to increase the number of leads that are directly connected to the chip.

This maximizes the thermal performance and increases the package area available for active silicon. Certain aspects of this technology are the subjects of a pending patent application.

The new 4-milliohm Si4430DY can handle up to 22 A of current and will dissipate up to 3.5 W, a nearly two-fold improvement over any previous power MOSFET in the SO-8 package. With power dissipation capabilities comparable to much larger devices, it will allow designers of Pentium II power conversion circuitry in desktop computers to replace the DPAK power MOSFETs now used in this application with the much smaller LITTLE FOOT SO-8 device. Current handling is so improved compared to previous-generation devices that the number of MOSFETs used as switching elements

can be cut in half.

Using the same packaging technology in a much smaller footprint, Vishay Siliconix is also offering two p-channel devices for bidirectional blocking battery disconnect applications. The new Si3801DV and Si3803DV are the first products on the market to provide a complete reverse blocking function with two MOSFETs in a LITTLE FOOT TSOP-6, allowing designers to implement dual battery systems with a package measuring just 3.02 x 2.84 x 1.01 mm. These new devices will allow manufacturers to provide this useful feature more affordably, and with less board space, than was ever before possible.

The new Si3801DV and Si3803DV provide the industry's lowest on-resistance for a p-channel battery switch in this package type, just 250 milliohm total for both MOSFETs in series. For very low-voltage systems, the Si3803DV is specified for operation at gate drives as low as 1.8 V. Vishay Siliconix is the industry's first supplier to offer power MOSFETs with a 1.8-V operating voltage. An additional 12 such devices, which are essential components in the development of ultra-low-voltage portable systems, are being separately released by Vishay Siliconix.

Samples of the Si4430DY, Si3801DV, and Si3803DV are available now. Production quantities are available in Q4 1998 for the Si3801DV and Si3803DV, and in Q1 1999 for the Si4430DY.

Siliconix (NASDAQ: "SILI"), a company of Vishay Intertechnology, Inc., is a leading manufacturer of power MOSFETs, power ICs, and analog signal processing devices for computers, cell phones, fixed communications networks, automobiles, and other electronic systems. With 1997 worldwide sales of $322 million, the Company's facilities include Class 1, six-inch wafer fabs dedicated to the manufacture of power products in Santa Clara, California and Itzehoe, Germany. Analog switches, analog multiplexers, and low-power transistors are fabricated in the Company's four-inch wafer fab in Santa Clara and by a subcontractor in Beijing, China. Assembly and test facilities include a Company-owned facility in Taiwan, a joint venture in Shanghai, China, and subcontractors in the Philippines, India, and Taiwan.

Vishay Intertechnology, Inc. (NYSE: VSH), a Fortune 1,000 company with revenues running at an annual rate of approximately $1.6 billion, is the largest U.S. and European manufacturer of passive electronic components (resistors, capacitors, inductors) and a major producer of discrete semiconductors (diodes, optoelectronics, transistors), IrDCs and power ICs. The company's components are vital to the operation of everything electronic and can be found in products produced by virtually all U.S. and European electronics equipment manufacturers. With headquarters in Malvern, Pennsylvania, Vishay employs over 20,000 people in over 60 facilities in the U.S., Mexico, Germany, Austria, Hungary, the United Kingdom, France, Portugal, the Czech Republic, Israel, Japan, Taiwan, China and the Philippines.

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